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CBTU0808

Dual lane PCI Express port multiplexer

Rev. 01 — 2 June 2006 Product data sheet

1. General description

The CBTU0808 is a dual lane port multiplexer designed to provide convenient and reliable path switching for PCI Express signals. It is organized as two PCI Express lanes, each consisting of a Transmit and Receive channel. Each channel has four ports, two (A and B) on the source (or host) side and two (A and B) on the destination (or device) side. Each port provides a pair of signal lines to support PCIe differential signaling.

Using specially designed high-bandwidth and high off-isolation switch elements, source and destination ports can be connected or isolated in three possible configurations: source A and B to destinations A and B respectively; or source A to destination B (remaining ports isolated), or all ports isolated.

The switch elements are controlled by internal control logic to set switch positions in accordance with these three configurations, selectable by CMOS inputs CTRL0 and CTRL1 for lanes 0 and 1 respectively. Within a lane, the switch configuration is always applied identically to both transmit and receive channels.

The CBTU0808 is packaged in a 48-ball, depopulated 9 × 9 grid, 0.5 mm ball pitch, thin profile fine-pitch ball grid array (TFBGA) package, which (while requiring a minimum 5 mm × 5 mm of board space) allows for adequate signal routing and escape using conventional board technology.

2. Features

- 2-lane wide PCI Express port multiplexer
- One transmit and one receive differential channel per lane
- Four ports per channel
- PCI Express signaling compliant
- High bandwidth: > 1 GHz
- Low OFF-feedthrough of < –35 dB at 1.25 GHz
- Low channel crosstalk of < –35 dB at 1.25 GHz
- Designed to match characteristic impedance of PCIe signaling environment
- Single 1.8 V supply operation
- ESD resilience of 2 kV HBM
- Available in 48-ball, 5 mm × 5 mm, 0.5 mm ball pitch TFBGA package, Pb-free/Green

3. Applications

- High-performance computing applications
- Port switching and docking applications

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4. Ordering information

Table 1. Ordering information

Type number	Solder process	Package		
		Name	Description	Version
CBTU0808EE/G	Pb-free (SnAgCu solder ball compound)	TFBGA48	plastic thin fine-pitch ball grid array package; 48 balls; body 5 × 5 × 0.8 mm	SOT918-1

5. Functional diagram

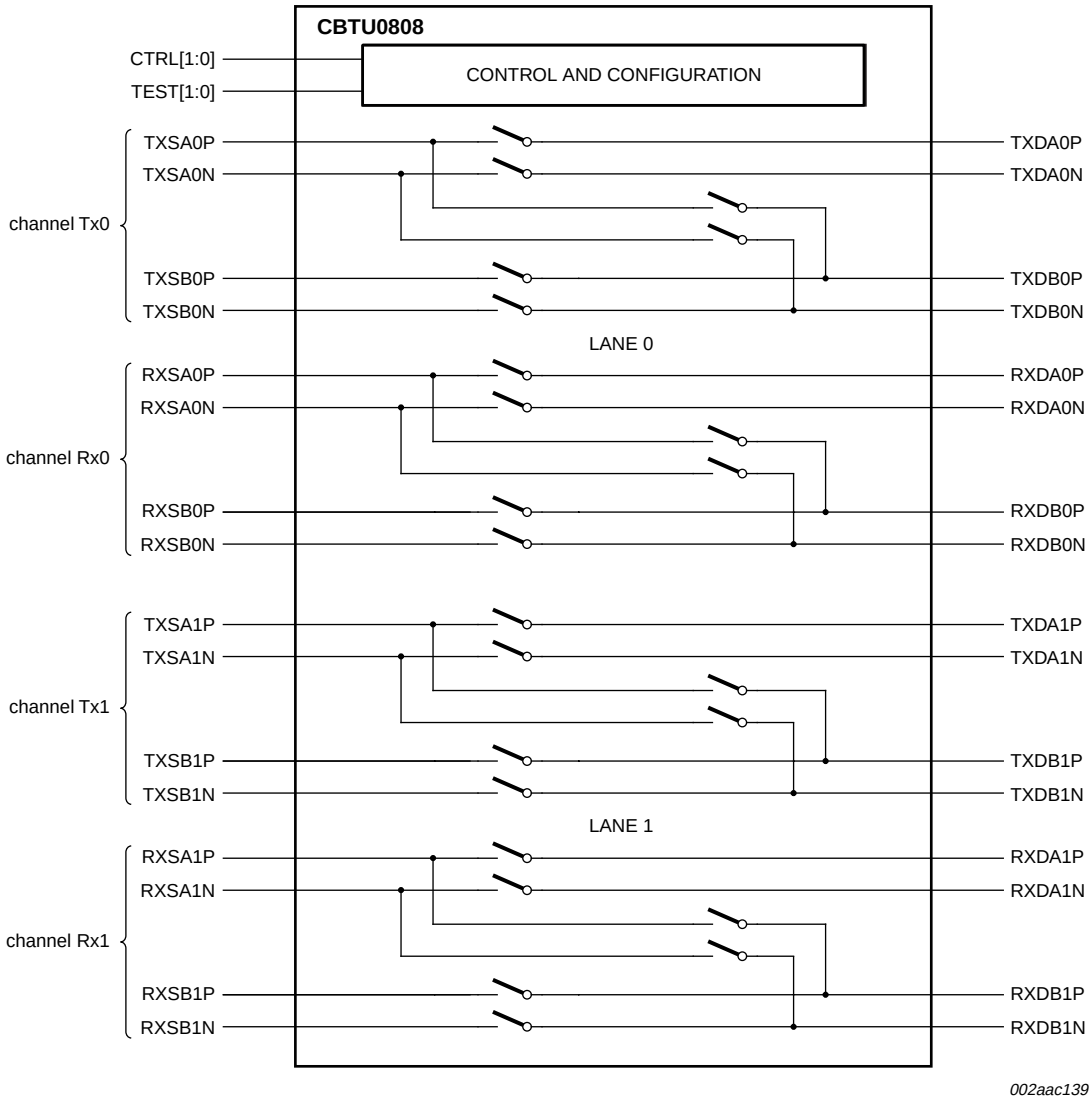

Fig 1. Functional diagram

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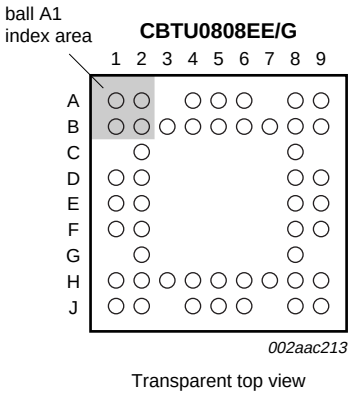
6. Pinning information

6.1 Pinning



Transparent top view

Fig 2. Pin configuration for TFBGA48

	1	2	3	4	5	6	7	8	9
A	CTRL0	TXSB0P		TXSA0P	GND	TXDA0P		TXDB0P	TEST1
B	RXSA0P	GND	TXSB0N	TXSA0N	V_{DD}	TXDA0N	TXDB0N	GND	RXDA0P
C		RXSA0N						RXDA0N	
D	RXSB0P	RXSB0N						RXDB0N	RXDB0P
E	GND	V_{DD}						V_{DD}	GND
F	TXSA1P	TXSA1N						TXDA1N	TXDA1P
G		TXSB1N						TXDB1N	
H	TXSB1P	GND	RXSA1N	RXSB1N	V_{DD}	RXDB1N	RXDA1N	GND	TXDB1P
J	TEST0	RXSA1P		RXSB1P	GND	RXDB1P		RXDA1P	CTRL1

002aac212

48-ball, 9 × 9 grid; top view. An empty cell indicates no ball is populated at that grid point.

Fig 3. Ball mapping

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6.2 Pin description

Table 2. Pin description

Signal group	Symbol	Pin	Type	Description
Test and control	CTRL0	A1	CMOS input	Switch configuration control inputs. See Table 3 “Switch configuration truth table”.
	CTRL1	J9		
	TEST0	J1	CMOS input	Test input. Used for test purposes only. Should be left open-circuit during normal operation. An internal pull-down resistor will default this pin to a LOW state.
	TEST1	A9	output	Test output. Used for test purposes only. Should be left open-circuit in normal application.
Signal ports	TXSA0P, TXSA0N, TXSB0P, TXSB0N	A4, B4, A2, B3	signal port	Transmit ports A and B differential signal terminals for Lane 0, Source side.
	RXSA0P, RXSA0N, RXSB0P, RXSB0N	B1, C2, D1, D2	signal port	Receive ports A and B differential signal terminals for Lane 0, Source side.
	TXSA1P, TXSA1N, TXSB1P, TXSB1N	F1, F2, H1, G2	signal port	Transmit ports A and B differential signal terminals for Lane 1, Source side.
	RXSA1P, RXSA1N, RXSB1P, RXSB1N	J2, H3, J4, H4	signal port	Receive ports A and B differential signal terminals for Lane 1, Source side.
	TXDA0P, TXDA0N, TXDB0P, TXDB0N	A6, B6, A8, B7	signal port	Transmit ports A and B differential signal terminals for Lane 0, Destination side.
	RXDA0P, RXDA0N, RXDB0P, RXDB0N	B9, C8, D9, D8	signal port	Receive ports A and B differential signal terminals for Lane 0, Destination side.
	TXDA1P, TXDA1N, TXDB1P, TXDB1N	F9, F8, H9, G8	signal port	Transmit ports A and B differential signal terminals for Lane 1, Destination side.
	RXDA1P, RXDA1N, RXDB1P, RXDB1N	J8, H7, J6, H6	signal port	Receive ports A and B differential signal terminals for Lane 1, Destination side.
Power	V_{DD}	B5, E2, E8, H5	power	power supply pins
	GND	A5, B2, B8, E1, E9, H2, H8, J5	power	ground pins

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7. Functional description

7.1 Functional description

7.1.1 General information

The CBTU0808 Dual lane PCI Express port multiplexer is designed to allow port switching of up to two PCI Express lanes (each including a Transmit and Receive channel) according to three switch configuration settings (described in Section 7.1.2.1). The basic switch element of the CBTU0808 is designed integrally with its package and chip interconnect to present an optimum characteristic on-impedance when used in a PCI Express signaling environment, and to provide high off-port isolation and low crosstalk.

7.1.2 Functional information

The following paragraphs describe the control and configuration possibilities available in the CBTU0808.

7.1.2.1 Switch configuration

The position of the port switches is controlled by CMOS input signals CTRL[1:0] and can be overridden by CMOS input TEST0 to disconnect (open) all ports between source and destination. For a given lane, the switch positions are always identical between transmit and receive channels. Lane 0 is controlled by CTRL0 and Lane 1 is controlled by CTRL1. The truth table for the switch position as a function of these inputs is shown in Table 3.

Table 3. Switch configuration truth table

Inputs		Function			
CTRLn[1]	**TEST0**	**Source ports[1]**	**Destination ports**		**Comment**
			A	**B**	
LOW	LOW	An	R_{on}	high-Z	SA:DA/SB:DB (Dual Through mode)
		Bn	high-Z	R_{on}	
HIGH[2]	LOW	An	high-Z	R_{on}	SA:DB (Single Cross mode)
		Bn	high-Z	high-Z	
LOW	HIGH	An	high-Z	high-Z	All ports open-circuit (Disconnect mode)
		Bn	high-Z	high-Z	
> LOW	HIGH	Test mode for internal use only			do not use

[1] n is the Lane number (0 or 1).

[2] CTRL1 or CTRL0 = HIGH.

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8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage			–0.5	+2.5	V
V_I	input voltage		[1]	–0.5	+2.5	V
I_{IK}	input clamping current	$V_I < 0$ V or $V_I > V_{DD}$		-	–50	mA
I_{OK}	output clamping current	$V_O < 0$ V or $V_O > V_{DD}$		-	±50	mA
I_O	output current	continuous; 0 V < V_O < V_{DD}		-	±50	mA
I_{CCC}	continuous current through each V_{DD} or GND pin			-	±100	mA
T_{stg}	storage temperature			–65	+150	°C
V_{esd}	electrostatic discharge voltage	Human Body Model; 1.5 kΩ; 100 pF		>2	-	kV
		Machine Model; 0 Ω; 200 pF		>200	-	V

[1] The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

9. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DD}	supply voltage			1.7	-	1.9	V
V_I	input voltage	TXn and RXn ports		–0.25	-	+1.75	V
V_{IH}	HIGH-level input voltage	CTRL[1:0], TEST inputs	[1]	0.65 × V_{DD}	-	V_{DD}	V
V_{IL}	LOW-level input voltage	CTRL[1:0], TEST[1:0] inputs	[1]	-	-	0.35 × V_{DD}	V
V_{ICR}	common mode input voltage range	TXn and RXn ports		0	-	1.5	V
$V_{I(dif)(p-p)}$	peak-to-peak differential input voltage	TXn and RXn ports	[2]	-	-	1.2	V
T_{amb}	ambient temperature	operating in free air		0	-	+85	°C

[1] The CTRL[1:0] inputs of the device must be held at valid levels (not floating) to ensure proper device operation.

[2] $V_{I(dif)(p-p)} = 2 \times |V_{TX_D+} - V_{TX_D-}|$. See Paragraph 4.3.3, Table 4-5 of Ref. 1.

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10. Static characteristics

Table 6. Static characteristics

Over recommended operating conditions, unless otherwise noted.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{DD}	supply current		[1]	-	-	1	mA
Digital inputs CTRL[1:0] and TEST0							
I_{LI}	input leakage current	$V_I = V_{DD}$ or GND		-	-	±5	µA
C_i	input capacitance	$V_I = V_{DD}$ or GND		-	-	5	pF
Signal ports TXSA0P … RXDB1N							
I_{LI}	input leakage current	$V_I = V_{DD}$ or GND; TEST0 = HIGH (Disconnect mode)		–100	-	+100	µA
$R_{on(sw)}$	switch on-state resistance			8	10	12	Ω
$\Delta R_{on(sw)}$	switch on-state resistance variation	over recommended V_{ID} (input voltage) range		-	0.5	0.75	Ω
$C_{S(ON)}$	ON-state capacitance	V_I = 0.9 V					
		switch; simulated value of the silicon switch only, excluding package parasitics		-	3.6	4.75	pF

[1] Static operating current.

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11. Dynamic characteristics

Table 7. Dynamic characteristics

Over recommended operating conditions, unless otherwise noted. Characterization bandwidth: 10 MHz < f_{oper} < 6 GHz.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{PD}	propagation delay	Figure 5	-	60	-	ps
$t_{startup}$	start-up time	supply voltage valid to switch specified operating characteristics	-	-	100	µs
t_{rcfg}	reconfiguration time	CTRL[1:0], TEST0 setting change to switch specified operating characteristics	-	-	100	µs
$t_{sk(o)}$	output skew time	difference in propagation delay between any two 'ON' paths within a channel; Figure 6	-	-	40	ps
$t_{sk(edge)}$	edge skew time	difference of rising edge propagation delay to falling edge propagation delay; Figure 7	-	-	40	ps
$t_{sk(dif)}$	differential skew time	difference in propagation delay between two members of a differential pair; Figure 8	-	-	5	ps
s_{12}	reverse transmission coefficient	Differential mode ON insertion loss; ON-state				
		f = 50 MHz	–0.8	-	-	dB
		f = 625 MHz	–2	-	-	dB
		f ≤ 1.25 GHz	–3.3	-	-	dB
s_{21}	forward transmission coefficient	Differential mode ON insertion loss; ON-state				
		f = 50 MHz	–0.8	-	-	dB
		f = 625 MHz	–2	-	-	dB
		f ≤ 1.25 GHz	–3.3	-	-	dB
s_{11}	input reflection coefficient	Differential mode ON return loss; ON-state				
		f = 50 MHz	-	-	–20	dB
		f = 625 MHz	-	-	–8	dB
		f ≤ 1.25 GHz	-	-	–6.0	dB
s_{22}	output reflection coefficient	Differential mode ON return loss; ON-state				
		f = 50 MHz	-	-	–20	dB
		f = 625 MHz	-	-	–8	dB
		f ≤ 1.25 GHz	-	-	–6.0	dB
s_{12}	reverse transmission coefficient	Differential mode port-to-port crosstalk; ON/OFF-state				
		f = 50 MHz	-	-	–35	dB
		f = 625 MHz	-	-	–35	dB
		f = 1.25 GHz	-	-	–35	dB
s_{21}	forward transmission coefficient	Differential mode port-to-port crosstalk; ON/OFF-state				
		f = 50 MHz	-	-	–35	dB
		f = 625 MHz	-	-	–35	dB
		f = 1.25 GHz	-	-	–35	dB

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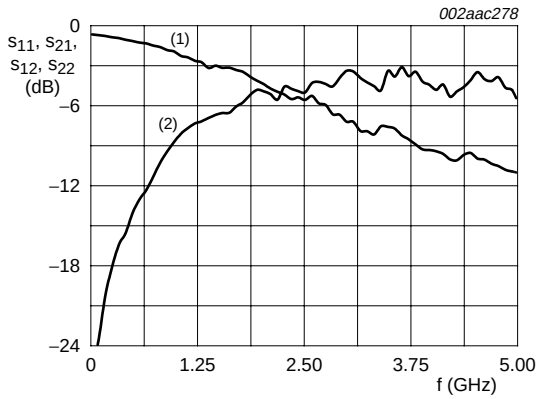
Table 7. Dynamic characteristics *…continued*

Over recommended operating conditions, unless otherwise noted. Characterization bandwidth: 10 MHz < f_{oper} < 6 GHz.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
S_{12}	reverse transmission coefficient	Differential mode off-port feedthrough; OFF-state				
		f = 50 MHz	-	-	–35	dB
		f = 625 MHz	-	-	–35	dB
		f = 1.25 GHz	-	-	–35	dB
S_{21}	forward transmission coefficient	Differential mode off-port feedthrough; OFF-state				
		f = 50 MHz	-	-	–35	dB
		f = 625 MHz	-	-	–35	dB
		f = 1.25 GHz	-	-	–35	dB



(1) insertion loss

(2) return loss

Fig 4. S parameters

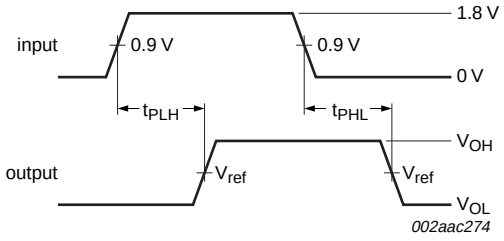


Fig 5. Propagation delay

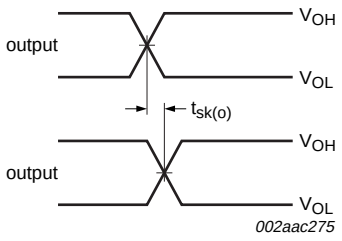


Fig 6. Output skew

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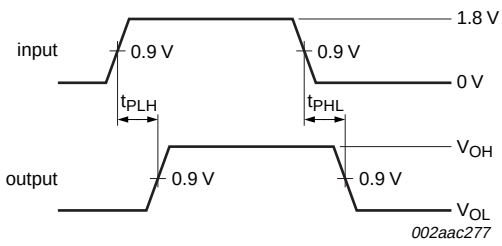


$t_{sk(edge)}$ =
$|t_{sk(edge)}$ rising $- t_{sk(edge)}$ falling$|$

Fig 7. Edge skew

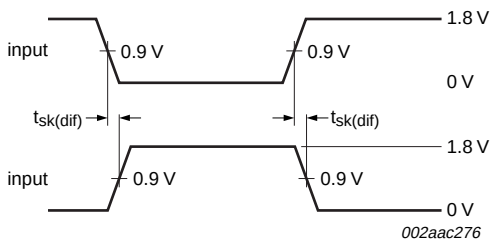
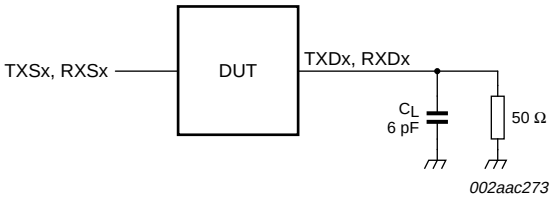


Fig 8. Differential skew

12. Test information



C_L represents board and jig and does not indicate additional capacitance.

All input pulses are supplied by generators having the following characteristics:
PRR ≤ 10 MHz; Z_o = 50 Ω; slew rate = 2.5 V/ns

Fig 9. Test circuit

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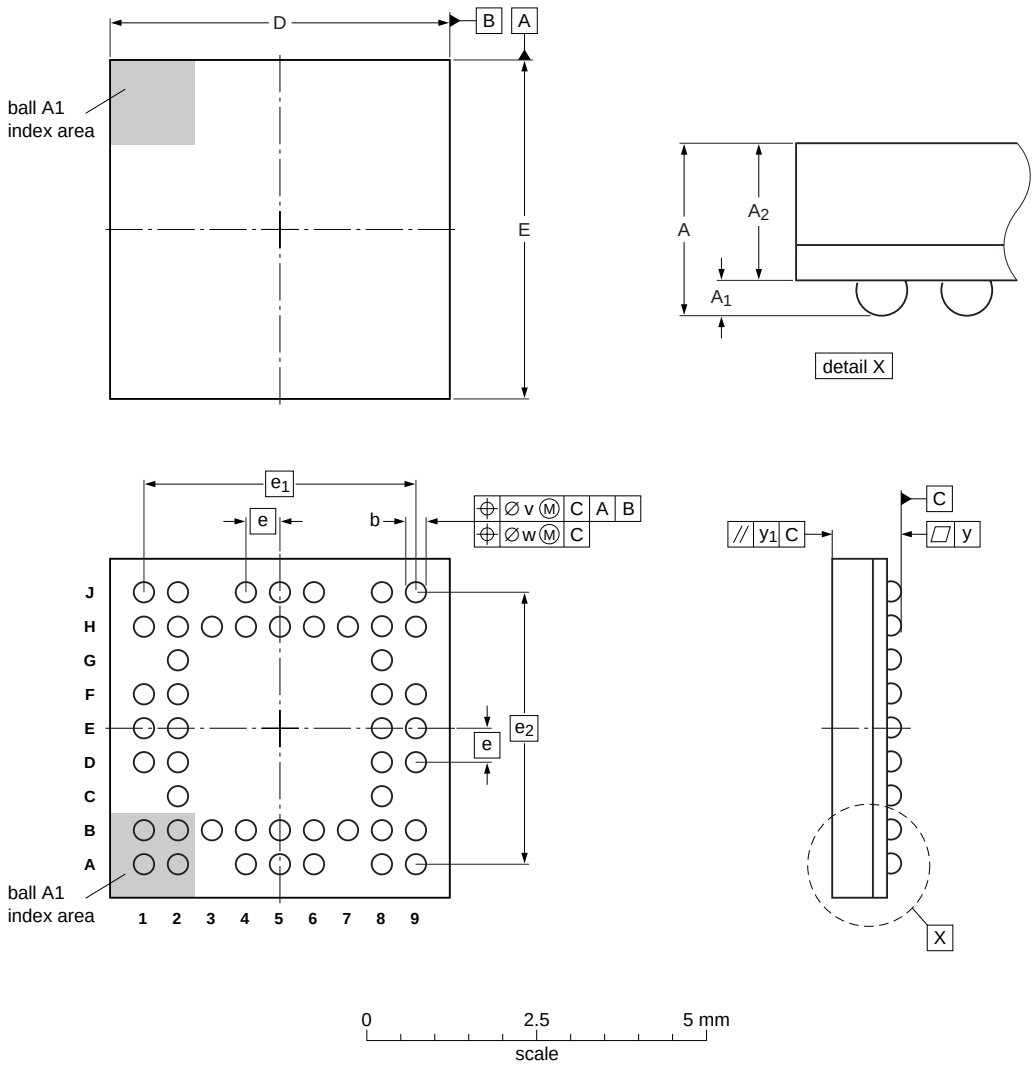
13. Package outline

TFBGA48: plastic thin fine-pitch ball grid array package; 48 balls; body 5 x 5 x 0.8 mm **SOT918-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
mm	1.15	0.25 0.15	0.90 0.75	0.35 0.25	5.1 4.9	5.1 4.9	0.5	4	4	0.15	0.05	0.08	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT918-1	- - -	MO-195	- - -			~~05-09-21~~ 05-10-13

Fig 10. Package outline SOT918-1 (TFBGA48)

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14. Soldering

14.1 Introduction to soldering surface mount packages

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

14.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 seconds and 200 seconds depending on heating method.

Typical reflow temperatures range from 215 °C to 260 °C depending on solder paste material. The peak top-surface temperature of the packages should be kept below:

Table 8. SnPb eutectic process - package peak reflow temperatures (from *J-STD-020C* July 2004)

Package thickness	Volume mm^3 < 350	Volume mm^3 ≥ 350
< 2.5 mm	240 °C + 0/–5 °C	225 °C + 0/–5 °C
≥ 2.5 mm	225 °C + 0/–5 °C	225 °C + 0/–5 °C

Table 9. Pb-free process - package peak reflow temperatures (from *J-STD-020C* July 2004)

Package thickness	Volume mm^3 < 350	Volume mm^3 350 to 2000	Volume mm^3 > 2000
< 1.6 mm	260 °C + 0 °C	260 °C + 0 °C	260 °C + 0 °C
1.6 mm to 2.5 mm	260 °C + 0 °C	250 °C + 0 °C	245 °C + 0 °C
≥ 2.5 mm	250 °C + 0 °C	245 °C + 0 °C	245 °C + 0 °C

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

14.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):

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- larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
- smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 seconds to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

14.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 seconds to 5 seconds between 270 °C and 320 °C.

14.5 Package related soldering information

Table 10. Suitability of surface mount IC packages for wave and reflow soldering methods

Package[1]	Soldering method	
	Wave	Reflow[2]
BGA, HTSSON..T[3], LBGA, LFBGA, SQFP, SSOP..T[3], TFBGA, VFBGA, XSON	not suitable	suitable
DHVQFN, HBCC, HBGA, HLQFP, HSO, HSOP, HSQFP, HSSON, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable[4]	suitable
PLCC[5], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[5][6]	suitable
SSOP, TSSOP, VSO, VSSOP	not recommended[7]	suitable
CWQCCN..L[8], PMFP[9], WQCCN..L[8]	not suitable	not suitable

[1] For more detailed information on the BGA packages refer to the *(LF)BGA Application Note* (AN01026); order a copy from your Philips Semiconductors sales office.

[2] All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods*.

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[3] These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding 217 °C ± 10 °C measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.

[4] These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.

[5] If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.

[6] Wave soldering is suitable for LQFP, QFP and TQFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.

[7] Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

[8] Image sensor packages in principle should not be soldered. They are mounted in sockets or delivered pre-mounted on flex foil. However, the image sensor package can be mounted by the client on a flex foil by using a hot bar soldering process. The appropriate soldering profile can be provided on request.

[9] Hot bar soldering or manual soldering is suitable for PMFP packages.

15. Abbreviations

Table 11. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
PCI	Peripheral Component Interconnect
PCIe	PCI Express
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
PRR	Pulse Repetition Rate
MM	Machine Model

16. References

[1] PCI Express Base Specification, Rev 1.1 — Revision 1.1, March 2005.

17. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
CBTU0808_1	20060602	Product data sheet	-	-

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18. Legal information

18.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.semiconductors.philips.com.

18.2 Definitions

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